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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/590,412	08/23/2006	Jean Brun	295350US2PCT	8749

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EXAMINER	
ROMAN, ANGEL	
ART UNIT	PAPER NUMBER
2812	

NOTIFICATION DATE	DELIVERY MODE
06/27/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/590,412	BRUN ET AL.	
	Examiner	Art Unit	
	ANGEL ROMAN	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 August 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/23/06, 11/21/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 13-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Oh et al. US Patent 6959856 filed 01/10/2003

Regarding claim 13, Oh et al. discloses a method to produce conductive rods (611) on an electronic component comprising one or more conductive blocks (602), each of the conductive rods (611) being in at least partial contact with a block (602) of the electronic component, the method comprising: deposition of a conductive base (606, 607) on the component (see figure 6a); deposition of a masking layer (615) on the conductive base (606, 607); formation in the masking layer (615) of a plurality of holes (616), at least one conductive block (602) of the conductive blocks (602) being located opposite one or more holes (616) (see figure 6b); filling of the holes with a conductive material base (611), by electrolysis and using the conductive base as an electrode, to form the conductive rods (see column 5, lines 32-36); and removal of the masking layer (615) (see figure 6e).

Regarding claim 14, Oh et al. discloses in the formation in the masking layer (615) of a plurality of holes (616), at least one conductive block (602) of the conductive blocks (602) is located opposite one or more holes (616), at least one hole (616) of the holes (616) has none of the conductive blocks (602) opposite it (see figure 6b), and the method further comprising, after the formation of the plurality of holes and prior to the filling by electrolysis: etching the conductive base via the holes (the conductive base is going to be at least partially etch via the holes immediately after the holes (616) are formed as a consequence of the etching process performed to form the holes 616) .

Regarding claim 15, Oh et al. discloses the masking layer comprising at least one photosensitive polymer (photoresist) layer (615).

Regarding claim 16, Oh et al. discloses the conductive blocks (602) being inserted in a passivation layer (6004) coating the electronic components (see figure 6a).

Regarding claim 17, Oh et al. discloses the conductive base (606, 607) being formed from a stack of at least two different conductive layers (606, 607).

Regarding claim 18, Oh et al. discloses after the masking layer removal, an at least partial conductive base removal or selective conductive base etching (see figure 6f).

Regarding claim 19, Oh et al. discloses, after the filling by electrolysis, an additional noble metal-based (605) chemical deposition on the conductive rods (611).

Regarding claim 20, Oh et al. discloses a microelectronic device obtained by the method according to claim 14 (see figure 6g).

Regarding claim 21, Oh et al. discloses, in the formation in the masking layer of a plurality of holes (616), at least one conductive block (602) of the conductive blocks (602) is located opposite one or more holes (616), at least one hole (616) of the holes

(616) has none of the conductive blocks (602) opposite it (see figure 6c), the method further comprising, between the deposition of the conductive base (606, 607) on the component and the deposition of the masking layer (615) on the conductive base: deposition of a thin insulating layer (603) on the conductive base (see figure 5a); and formation of a plurality of openings in the thin insulating layer (603), each opening being located opposite a conductive block (602) (see figure 6a).

Regarding claim 22, Oh et al. discloses the masking layer comprising at least one photosensitive polymer (photoresist) layer (615).

Regarding claim 23, Oh et al. discloses the conductive blocks (602) being inserted in a passivation layer (6004) coating the electronic components (see figure 6a).

Regarding claim 24, Oh et al. discloses the conductive base (606, 607) being formed from a stack of at least two different conductive layers (606, 607).

Regarding claim 25, Oh et al. discloses after the masking layer removal, an at least partial conductive base removal or selective conductive base etching (see figure 6f).

Regarding claim 26, Oh et al. discloses, after the filling by electrolysis, an additional noble metal-based (605) chemical deposition on the conductive rods (611).

Regarding claim 27, Oh et al. discloses a microelectronic device obtained by the method according to claim 14 (see figure 6g).

Regarding claim 28, Oh et al. discloses wherein, of the plurality of holes (616) formed in the hole formation in the masking layer (615), some holes reveal the thin insulating layer (603), and some other holes reveal the conductive base (606, 607).

Regarding claim 29, Oh et al. discloses the formation in the masking layer (615) of a plurality of holes (616), each hole (616) is at least partially located opposite a conductive block (602).

Regarding claim 30, Oh et al. discloses, after the formation in the masking layer (615) of a plurality of holes (616) and prior to the filling by electrolysis: etching of the conductive base via the holes (the conductive base is going to be at least partially etch via the holes immediately after the holes (616) are formed as a consequence of the etching process performed to form the holes 616).

Regarding claim 31, Oh et al. discloses the masking layer comprising at least one photosensitive polymer (photoresist) layer (615).

Regarding claim 32, Oh et al. discloses the conductive blocks (602) being inserted in a passivation layer (6004) coating the electronic components (see figure 6a).

Regarding claim 33, Oh et al. discloses the conductive base (606, 607) being formed from a stack of at least two different conductive layers (606, 607).

Regarding claim 34, Oh et al. discloses after the masking layer removal, an at least partial conductive base removal or selective conductive base etching (see figure 6f).

Regarding claim 35, Oh et al. discloses, after the filling by electrolysis, an additional noble metal-based (605) chemical deposition on the conductive rods (611).

Regarding claim 36, Oh et al. discloses a microelectronic device obtained by the method according to claim 14 (see figure 6g).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lu et al., Kim et al., Jeong et al., Ha et al., Hirano et al. and Gurtler et al. disclose method of forming conductive rods on conductive base opposite conductive blocks.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANGEL ROMAN whose telephone number is (571)272-6369. The examiner can normally be reached on IFP Mo-Fr 6am-3pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles D Garber can be reached on (571) 272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. R./
Examiner, Art Unit 2812
June 20, 2008

/Charles D. Garber/
Supervisory Patent Examiner, Art Unit 2812